What is claimed is:

1. An adaptive sigma delta modulator comprising:

a) an input stage that produces a difference signal representing the difference between an analog input signal x(n) and an analog feedback signal z(n), the amplitude of the analog input signal x(n) within a first range [-a, +a];

b) an accumulator stage that produces an accumulated signal that is a function of an accumulation of the difference signal, the accumulator stage transforming the accumulation of the difference signal so as to increase average magnitude while ensuring instantaneous magnitude does not exceed a predetermined value;

c) a quantization stage that produces a quantized digital signal $y_0(n)$ representing the accumulated signal;

d) an adaptation stage, that based on the quantized digital signal $y_0(n)$ produces a digital output signal $z_0(n)$; and

e) a digital-to-analog converter stage that converts the digital output signal $z_0(n)$ to the analog feedback signal z(n)

2. The adaptive sigma delta modulator according to claim 1, wherein the adaptation stage tends to keep the instantaneous magnitude of the analog feedback signal z(n) within the first range [-a, +a] and greater than the analog input signal's x(n) instantaneous magnitude.

3. The adaptive sigma delta modulator according to claim 1, wherein the accumulator stage includes an accumulation capacitor, the charge across the accumulation capacitor representing the accumulation of the difference signal.

4. The adaptive sigma delta modulator according to claim 3, wherein the accumulated signal is based, at least in part, on the voltage across the accumulation capacitor.

5. The adaptive sigma delta modulator according to claim 3, wherein the capacitance across the accumulation capacitor is variably controlled such that average magnitude of voltage across the accumulation capacitor is increased while ensuring instantaneous magnitude of voltage across the accumulation capacitor does not exceed the predetermined value.

6. The adaptive sigma delta modulator according to claim 3, wherein the accumulation capacitor is coupled between an input and an output of an operational amplifier.

7. The adaptive sigma delta modulator according to claim 3, wherein the adaptation stage includes a multiplier stage that multiplies the quantized digital signal $y_0(n)$ by a step size $c_0(n)$, and wherein the capacitance across the accumulation capacitor is variably controlled based, at least in part, on the step size $c_0(n)$.

8. The adaptive sigma delta modulator according to claim 3, wherein the accumulation capacitor includes an array of capacitors, each capacitor in the array capable of being switched so as to vary the capacitance across the accumulation capacitor.

9. The adaptive sigma delta modulator according to claim 1, wherein the digital-to-analog converter includes an array of weighted capacitors, the array of weighted capacitors capable of acquiring a charge $Q_{DAC}(n)$ negatively proportional to the digital output signal $z_0(n)$.

10. The adaptive sigma delta modulator according to claim 1, wherein the input sampling stage includes an input sampling capacitor, the input sampling capacitor capable of acquiring a charge $Q_{in}(n)$ proportional to the analog input signal $x(n)$.

11. A method of adapting sigma delta modulation, the method comprising:

a) producing a difference signal representing the difference between an analog input signal $x(n)$ and an adaptive feedback signal $z(n)$, the amplitude of the analog input $x(n)$ within a first range $[-a, +a]$;

b) producing an accumulated signal that is a function of an accumulation of the difference signal, wherein producing the accumulated signal includes transforming the accumulation of the difference signal so as to increase average magnitude while ensuring instantaneous magnitude does not exceed a predetermined value;

c) producing a quantized digital signal $y_0(n)$ representing a quantization of the accumulated signal;

d) producing a digital output signal $z_0(n)$ based on the quantized digital signal $y_0(n)$; and

e) performing a digital-to-analog conversion on the digital output signal $z_0(n)$ to produce the adaptive feedback signal z(n).

12. The method according to claim 11, wherein producing a digital output signal $z_0(n)$ includes keeping the instantaneous magnitude of the analog feedback signal z(n) within the first range [-a, +a] and greater than the analog input signal's x(n) instantaneous magnitude

13. The method according to claim 11, wherein producing the accumulated signal includes storing charge across an accumulation capacitor, the charge representing the accumulation of the difference signal.

14. The method according to claim 13, wherein producing the accumulated signal includes variably controlling capacitance across the accumulation capacitor.

15. The method according to claim 14, wherein variably controlling capacitance across the accumulation capacitor includes variably controlling capacitance across the accumulation capacitor so as to increase the average voltage across the accumulation capacitor while ensuring instantaneous voltage across the accumulation capacitor does not exceed the predetermined value.

16. The method according to claim 14, wherein producing the digital output signal $z_0(n)$ includes multiplying the quantized digital signal $y_0(n)$ by a step size $c_0(n)$ and wherein variably controlling capacitance across the accumulation capacitor includes varying the capacitance across the accumulation capacitor based, at least in part, on the step size $c_0(n)$.

17. The method according to claim 13, wherein the accumulation capacitor is coupled between an input and an output of an operational amplifier.

18. The method according to claim 13, wherein the accumulation capacitor includes an array of capacitors, and wherein variably controlling capacitance across the accumulation capacitor includes switching at least one capacitor in the array so as to vary the capacitance across the accumulation capacitor.

19. The method according to claim 18, wherein switching at least one capacitor in the array includes disconnecting at least one capacitor in the array so as to decrease the capacitance across the accumulation capacitor.

20. The method according to claim 18, wherein switching at least one capacitor in the array includes activating at least one capacitor in the array so as to increase the capacitance across the accumulation capacitor.

21. The method according to claim 14, wherein variably controlling capacitance across the accumulation capacitor includes losing substantially no charge across the accumulation capacitor.

22. The method according to claim 11, wherein performing the digital-to-analog conversion on the digital output signal $z_0(n)$ to produce the adaptive feedback signal z(n) includes acquiring a charge $Q_{DAC}(n)$ on an array of weighted capacitors, the charge $Q_{DAC}(n)$ negatively proportional to the digital output signal $z_0(n)$.

23. The method according to claim 11, wherein producing the difference signal includes acquiring a charge $Q_{in}(n)$ on an input sampling capacitor, the charge $Q_{in}(n)$ proportional to the analog input signal x(n).

24. An adaptive sigma delta modulator comprising:

a) an input stage that produces a difference signal representing the difference between an analog input signal x(n) and an analog feedback signal z(n), the amplitude of the analog input signal x(n) within a first range [-a, +a];

b) an accumulator stage that produces an accumulated signal that is a function of an accumulation of the difference signal, the accumulator stage including an accumulation capacitor, the charge across the accumulation capacitor representing the accumulation of the difference signal, the capacitance across the accumulation capacitor capable of being variably controlled;

c) a quantization stage that produces a quantized digital signal $y_0(n)$ representing the accumulated signal;

d) an adaptation stage, that based on the quantized digital signal $y_0(n)$ produces a digital output signal $z_0(n)$; and

e) a digital-to-analog converter stage that converts the digital output signal $z_0(n)$ to the analog feedback signal z(n).

25. The adaptive sigma delta modulator according to claim 24, wherein the accumulation capacitor is variably controlled so as to increase the average magnitude of the voltage across the accumulation capacitor while ensuring an instantaneous magnitude of the voltage across the accumulation capacitor does not exceed a predetermined value.

26. The adaptive sigma delta modulator according to claim 24, wherein the accumulation capacitor includes an array of capacitors, each capacitor in the array capable of being switched so as to vary the capacitance across the accumulation capacitor.

27. The adaptive sigma delta modulator according to claim 24, wherein the adaptation stage includes a multiplier stage that multiplies the quantized digital signal $y_0(n)$ by a step size $c_0(n)$, and wherein the capacitance across the accumulation capacitor is variably controlled based, at least in part, on the step size $c_0(n)$.

28. The adaptive sigma delta modulator according to claim 24, wherein the adaptation stage tends to keep the instantaneous magnitude of the analog feedback signal z(n) within the first range [-a, +a] and greater than the analog input signal's x(n) instantaneous magnitude.

29. A method of adapting sigma delta modulation, the method comprising:

a) producing a difference signal representing the difference between an analog input signal x(n) and an adaptive feedback signal z(n), the amplitude of the analog input x(n) within a first range [-a, +a];

b) producing an accumulated signal that is a function of an accumulation of the difference signal, wherein producing the accumulated signal includes variably controlling capacitance across an accumulation capacitor, the charge across the accumulation capacitor representing an accumulation of the difference signal;

c) producing a quantized digital signal $y_0(n)$ representing a quantization of the accumulated signal;

d) producing a digital output signal $z_0(n)$ based on the quantized digital signal $y_0(n)$; and

e) performing a digital-to-analog conversion on the digital output signal $z_0(n)$ to produce the adaptive feedback signal z(n).

30. The method according to claim 29, wherein capacitance across the accumulation capacitor is variably controlled such that an average magnitude of voltage across the accumulation capacitor is increased while ensuring an instantaneous magnitude of voltage across the accumulation capacitor does not exceed a predetermined value.

31. The method according to claim 29, wherein producing the digital output signal $z_0(n)$ includes multiplying the quantized digital signal $y_0(n)$ by a step size $c_0(n)$ and wherein variably controlling capacitance across the accumulation capacitor includes varying the capacitance across the accumulation capacitor based, at least in part, on the step size $c_0(n)$.

32. The method according to claim 29, wherein producing the digital output signal $z_0(n)$ includes substantially keeping the instantaneous magnitude of the analog feedback signal z(n) within the first range [-a, +a] and greater than the analog input signal's x(n) instantaneous magnitude.

33. A sigma delta modulator comprising:

a) an input stage that produces a difference signal representing the difference between an analog input signal x(n) and an analog feedback signal z(n);

b) an accumulator stage that produces an accumulated signal that is a function of an accumulation of the difference signal, the accumulator stage transforming the accumulation of the difference signal so as to increase average magnitude while ensuring instantaneous magnitude does not exceed a predetermined value;

c) a quantization stage that produces a quantized digital signal $y_0(n)$ representing the accumulated signal; and

d) a digital-to-analog converter stage that converts the digital signal $y_0(n)$ to the analog feedback signal z(n).